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Research Article

The Silicon Age: Trends in Semiconductor Devices Industry

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Abstract

The semiconductor devices industry is one of the most significant sectors, based on its broad applications and substantial economic and strategic implications. This article overviews the emerging technologies in transistor manufacturing processes, materials, and architectures. It discusses the latest trends in photo-lithography processes, focusing on extreme ultraviolet (EUV) lithography; at the transistor architectural level, the article discusses various transistor types, emphasizing fin field-effect transistor (FinFET) structure and properties. The article also briefs the latest semiconductor developing road map, promises, and challenges toward keeping up with Moore's integration rate.

Keywords: EUV, FinFET, lithography, Silicon.

1. Introduction

In 1956, Bell Labs developed the solid-state transistor using Germanium (Ge). Later, Silicon (Si) replaced Ge for many reasons; Si readily interacts with oxygen (O_2), forming the SiO_2 layer, which functions as an electrical insulator. This layer is necessary for metal–oxide–semiconductor field-effect transistor (MOSFET), as it separates the gate from the channel and serves as a masking layer on junctions, preventing dopant diffusion in the region it shields. Si also has a higher potential difference between its conduction and valence band (band-gab), making Si less capable of thermal-pair production, which indicates that Si devices have less noise at the same temperature. At a p-n junction, Si has a lower reverse current (leakage current) and higher peak inverse voltage. Si crystals can withstand more heat than Ge. Furthermore, Si is found naturally in sand, and processing it is simpler and less expensive, all of which led to the designation of this era as 'The Silicon Age'.

The fabrication of the integrated circuits starts with forming thin wafers of pure crystalline Silicon. These wafers are commonly referred to as undoped or intrinsic silicon wafers. The electrical properties of Si can be fine-tuned by adding dopants. For example, p-type wafers are generated when silicon wafers are doped with impurities such as Boron, and n-type wafers are generated when silicon wafers are doped with Arsenic or Phosphorous. This article discusses the most recent semiconductor technologies, their fundamental characteristics, and the major manufacturing trends. Local Oxidation of Silicon (LOCOS) is a process that uses silicon dioxide to isolate neighboring components inside a silicon wafer to reduce electric current leakage (crosstalk). This isolation method is typically applied at 250 nm nodes or earlier complementary metal-oxide–semiconductor (CMOS) technologies. In modern techniques, shallow trench isolation (STI), also known as the box isolation method, is applied instead.

2. Semiconductors Industry Overview

Silicon is among the least expensive elements, but the industry turns it into one of the most valuable items, an integrated circuit (IC). All electronic devices, such as PCs, tablets, and smartphones, rely on semiconductor components; therefore, semiconductor processing technology is a must for war and peace. While China has the world's largest Silicon mining industry, each year, it imports about US$ 300 billion worth of ICs from the United States [1].

In 2019, 32.4% of the semiconductor market segment was for networks and communications devices. In 2021, the global semiconductor market is foreseen to hit US$ 469.4 billion, and the semiconductor's annual growth rate is predicted to be 8.4% and it is projected to reach US$ 726.73 billion by 2027 [2].

Advanced semiconductor materials lithography (ASML), a Philips spin-off located in the Netherlands, is one of the few companies that manufacture photo-lithography equipment capable of producing the most advanced microchips. Most western-world extreme ultraviolet lithography (EUL) development has been done in the virtual national laboratory (VNL), which comprises three labs, Lawrence Livermore national laboratory, Sandia national laboratories, and Lawrence Berkeley national laboratory. VNL research works helped ASML release its EUL machine (NXE:3400B) in 2017; it is capable of manufacturing 7-5 nm technologies with a thruput of 125 wafers per hour [3] and its successor (NXE:3400C) with a thruput of 170 wafers per hour, and develop the high-numerical-aperture lens (EXE:5000), which is planned for 2023 to achieve 3-2 nm [4]. In 2020, ASML's sales amounted to € 10.3 billion, of which 18% went to China, 36% to Taiwan, and 31% to South Korea; however, no EUV machine was shipped to China, as the EUV machines are based on US patents; thus ASML had to comply with the restrictions within the US entity lists [5], [6].

The alternative to EUV is to use sophisticated masks with advanced nanoimprint lithography (NIL) technologies; this enabled Kaixia in Japan to achieve sub-15 nm chips, with a

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goal of 5 nm by 2025. The ranks of the top 15 companies that manufacture optoelectronics, sensors, actuators, and discrete semiconductors (O-S-D) in 2019 and the forecasted (2020F) are shown in Table 1 [7]. In the third quarter of 2021, Taiwan Semiconductor Manufacturing Company (TSMC) held over 53% of the worldwide semiconductor foundry industry, while Samsung held 17.1% [8]. TSMC also plays a vital role in this techno-political issue and has responded to the US concerns about electronics chips shortage impact on various industries and the urge to strengthen the supply chain [9]; thus, TSMC started building a 12 billion chip plant in Arizona to start producing 5 nm chips by 2024 [10].

On the eastern side of the globe, China tries to catch up through its research centers, such as the Shanghai synchrotron radiation facility (SSRF), which announced in 2020 achieving a 25 nm half-pitch pattern using soft X-ray interference lithography (XIL). The main aim of these XIL experiments was to manufacture precise periodic patterns with higher resolution, more depth of focus, and higher thruput than the other high-resolution techniques, like electron beam lithography (EBL), focused ion beam (FIB), and NIL. Furthermore, XIL applies a non-contact exposure approach, extending the mask lifetime compared to NIL [11].

This article highlights the main specifications that make EUV superior to deep-ultraviolet (DUV) chip-making equipment. It also reviews other advances of nano-scale electronic devices in terms of achievements, challenges, and promises.

Table 1: 2020F Top 15 Semiconductor Sales Leaders (USD M, Including Foundries)

2020 Rank	2019 Rank	Company	H.Q.	2019 Total IC	2019 Total OSD	2019 Total Semi	2020F Total IC	2020F Total OSD	2020F Total Semi	2020 / 2019 %
1	1	Intel	U.S.	70,797	0	70,797	73,894	0	73,894	4%
2	2	Samsung	S. Korea	52,486	3,223	55,709	56,899	3,583	60,482	9%
3	3	TSMC (1)	Taiwan	34,668	0	34,668	45,420	0	45,420	31%
4	4	SK Hynix	S. Korea	22,578	607	23,185	25,499	971	26,470	14%
5	5	Micron	U.S.	22,405	0	22,405	21,659	0	21,659	-3%
6	7	Qualcomm (2)	U.S.	14,391	0	14,391	19,374	0	19,374	35%
7	6	Broadcom (2)	U.S.	15,521	1,722	17,243	15,362	1,704	17,066	-1%
8	10	Nvidia (2)	U.S.	10,618	0	10,618	15,884	0	15,884	50%
9	8	TI	U.S.	12,812	839	13,651	12,275	813	13,088	-4%
10	9	Infineon (3)	Europe	7,734	3,404	11,138	7,438	3,631	11,069	-1%
11	8	MediaTek (2)	Taiwan	7,972	0	7,972	10,781	0	10,781	35%
12	16	Kioxia	Japan	8,760	0	8,760	10,720	0	10,720	22%
13	14	Apple* (2)	U.S.	8,015	0	8,015	10,040	0	10,040	25%
14	15	ST	Europe	6,475	3,058	9,533	6,867	3,085	9,952	4%
15	11	AMD (2)	U.S.	6,731	0	6,731	9,519	0	9,519	41%
Top 15 Total				301,963	12,853	314,816	341,631	13,787	355,418	13%

(1) Foundry (2) Fabless (3) Includes aquired company's sales in 2019 and 2020 results

*Custom processor/ devices

3. Advances in Photo-Lithography

A semiconductor fabrication process is tightly related to optical physics, where lenses and mirrors are the primary components of any photo-lithography system. The resolution of an optical system is based on Ernest Abbe's law (1873), where resolution = minimum feature size = critical dimension (half pitch) = $k_1 \frac{\lambda}{NA}$. In other words, the half-pitch (HP) means that the finest possible details are within a dimension of approximately $\frac{\lambda}{NA}$. k_1 is the process factor, representing the collective influence of aberrations, illumination settings, resist chemistry, and other factors. λ is the wavelength, and NA is the numerical aperture of the lens, as the wafer sees. NA is a dimensionless number representing the range of

angles over which a system accepts or emits light [12]. Before EUV, scaling λ down was limited; thus, the earlier resolution enhancement trend was based on increasing NA and decreasing k_1. Alternatively, with EUV, if mirrors with very low NA are used, the collimated beam can be distorted (aberrated) or even truncated.

3.1. DUV Lithography

Using 193 nm steppers to fabricate smaller nodes, even as large as 45 nm, mostly requires additional resolution enhancement techniques (RETs) photo-lithography techniques, including 1) phase shift masking (PSM) by adding phase information to the mask; 2) off-axis illumination (OAI) to optimize the angles of light illuminating the mask; 3) source polarization to control of the polarization of the illumination; 4) source mask optimization (SMO); 5) optical proximity correction (OPC) to optimize the mask pattern shape [13]–[15]. In short, fabricating minor features using long-wave lithography requires more masks and produces less precise devices. One of the well-known ASML's DUV lithography machines is TWINSCAN NXT:1470 which utilizes 193 nm UV light wave, with projection optics of 0.93 NA Carl Zeiss Starlith of 4X reduction that can achieve a resolution of about 0.57 nm, and the machine's thruput is about 300 wafer per hour [16].

3.2. EUV Lithography

The earliest published research work on the possibility of using short waves like the soft X-ray for lithography was by Heuberger in 1983 [17], then by Hoh in 1985 [18]. A photo-lithography process is usually done within a level-10 clean room (less than ten dust particles within a cubic foot) in a semiconductors foundry (a.k.a. fab). The EUV lithography process uses 13.5 nm light. At that tiny wavelength, the light is absorbed (or reflected) by almost everything, including glass lenses, the transparent quart that conventional masks are made of, and even air; thus, instead of transmitting light through a mask, an EUV mask (reticle) is reflective, and the process uses mirrors to bounce the light onto the silicon wafer, all in a vacuum. Furthermore, because most photo-resist layer compounds are sensitive to short wavelengths, a fab is often illuminated with yellow lights. In the DUV process, the 193 nm UV comes from Argon Fluoride (ArF) laser, but for the EUV, laser-based UV lithography is not sufficient anymore; instead, EUV is emitted from the laser-produced plasma. A high-energy CO_2 laser (∼25 kW) is pulsed at a high ∼50 kHz rate and hits a molten tin (Sn) microdroplet (of ∼30 um diameter) into hot dense plasma. The electrons absorb the laser pulse energy, and when they come to rest at a lower energy level, they emit (∼92 eV) energy, which forms ∼13.5 nm EUV light, which is mirrored toward the photo-lithography mask [19]–[21].

The EUV light wave is absorbed in nanometers of solids and micrometers of gases; the gases problem was solved by vacuum operation, but the absorption of solids remains an outstanding issue. At wavelengths < 50 nm, all materials would have a reflection index of ∼1, making it challenging to reflect from one interface. Zeiss (previously Carl Zeiss) company made multi-layer coated mirrors (a.k.a. distributed Bragg reflectors) by alternating layers of high-Z and low-Z materials, where Z is the atomic number, and Mo/Si layers are among the common layers. Molybdenum layers are typically ∼3 nm thick, while the Silicon layers are ∼4 nm thick. This multi-layer combination is optimum for 13.4 nm wavelength, achieving 68.2% reflectance [22]. The EUV photons bounce off several multi-layer illumination mirrors to hit the mask, then bounce off several multi-layer projection mirrors to hit the semiconductor wafer. In 2018, Samsung announced the first EUV-based 7 nm low power plus (LPP) processor, Exynos 9825 used for Galaxy Note 10, saving 40% area, 50% power, and enhancing the performance by 20% [23].

3.3. High-NA EUV Lithography

On its road map, ASML plans to launch a high-NA for the 2 nm node in 2023, which helps the lithography process complete with a single pass (single mask pattern) compared to the multiple passes required by the 0.33 NA EUV process. That also requires reducing the mask's 3D effect (shadowing) and coping with contrast and photon shot noise. Although the ASML high-NA system is based on the same laser-produced plasma, Zeiss should build high-NA optics to serve as an anamorphic lens that generates uneven magnifications along two perpendicular axes. ASML must also overcome other obstacles, including resists, masks, stitching, source power, limited depths-of-focus at 0.55 NA, lens polarization, and cost. The new ASML system is larger, more complex but yields higher throughput [4].

3.4. X-Ray Lithography

Researchers believe that the next generation of photo-lithography would utilize X-ray to get wavelengths in the range of (0.7–1.2) nm through (1-1.8) keV photon energy. Unlike DUV and EUV lithography, which allows mirrors to achieve 4:1 optical reduction between the size of the mask and the wafer, X-Ray requires a 1:1 mask to wafer rate. X-ray lithography requires precise masks using advanced nano chemicals to create membranes that can stand such high frequencies for a substantial period [24].

4. Advances in Materials

Shrinking silicon-based transistors reaching an end makes materials scientists explore alternative elements. Carbon, which naturally comes in semiconducting forms, is a great candidate, and Carbon nanotube field-effect transistor (CNFET) is a promising device. However, growing Carbon nanotubes where they are needed is still under research; therefore, they are made separately then placed where required; furthermore, having Carbon nanotube-based devices with fewer variations and uniformly oriented. Another significant challenge compared to silicon devices is doping tiny Carbon nanotubes with metals to have negative and positive substrates. A recent collaboration between MIT and Analog Devices, Inc. yielded a 16-bit Carbon nanotube-based processor [25]. Rather than positioning a single tube where needed, researchers produced a silicon surface with metallic features that are large enough to allow several nanotubes to bridge the metal features. To remove the aggregates, they deposited a material layer on top of the nanotubes and then sonicated it down. The sonication removed the material with the aggregates without disturbing the beneath nanotubes; they then etched off the nanotubes, leaving them just where they were required. On top of the nanotubes, a layer of various coating of oxide was added, the properties of the oxides, combined with the various metals used to connect the nanotubes, would turn them into p- or n-type semiconductors. Advancing the semiconductor industry requires much more than developing finer optical lithography; it also requires advanced methodologies within the semiconductor wafer, such as coating processes, chemical mechanical planarization/polishing (CMP), deposition, ion

implantation, and other factors. Improved wafer processing also includes advancements in semiconductor surface interfaces to avoid degrading carrier mobility in tiny devices and straining techniques to increase mobility within the channel.

5. Advances in Transistor Structure

On the architectural level, there are various attempts to improve the structures of transistors (front-end-of-line (FEOL)), contacts (middle-of-line (MOL)), and wiring (back-end-of-line (BEOL)). This section briefly reviews the most dominant trends in the semiconductor industry.

Scaling the gate-length down increases the leakage current, as the threshold voltage reduces with the increase of the drain-to-source voltage, a phenomenon is known as drain-induced barrier lowering (DIBL), and other short channel effects (SCE) diminish the differences between ON and OFF states. The greater the gate-to-channel capacitance, the more the gate controls the channel, reducing the SCE. High-k gate-insulators help increase gate capacitance, but gate-length scaling below 28-25 nm wors SCE. Still, keeping DIBL ~100 mV/V requires an oxide thickness of ~1 nm. In summary, most FET designs strive for the highest (I_{ON}/I_{OFF}) ratio possible, which is with today's technologies is ~ 10^5.

5.1. FinFET

Using the third dimension as FinFET came into practice in 2011. The gate is on two, three, or four sides of the channel, or wrapped around it, as illustrated in Fig.1. FinFETs mitigate the resistance and capacitance problems of planar FETs, as shrinking the fin width allows better control for the gate over the channel and reduces SCE. The fin (height/width), known as the *aspect* ratio, increases with every technology evolution. The prior evolution tendency was reducing the channel length while keeping (L/W) ~ 2.5. Reducing the spacing between the fins causes the contact pitch to drop while raising the fin height maintains the current per layout area rate. Such a scaling downtrend will eventually have a fragile fin that is hard to manufacture; Additionally, when the fin width decreases, carrier mobility decreases owing to interface dispersion and quantum confinement [26].

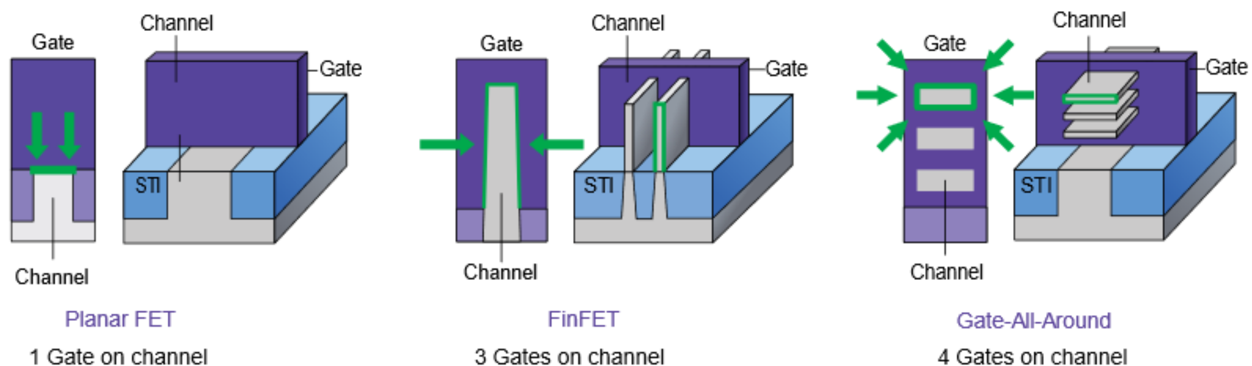

Fig. 1. Various MOSFET Types.

In the 2019 international electron devices meeting (IEDM), Ryckaert et al. from the interuniversity microelectronics center (IMEC) estimated smallest FinFET would have two fins, 5 nm apart, with a gate length of 15 nm [27]. A conventional cell has both an NFET and a PFET transistor, with the NFET and PFET transistors spaced optimally to reduce parasitic effects. The lithography method determines the minimum distance between fins and the need to install a gate metal and gate dielectric in between the fins. If the contact pitch is reduced, there would not be enough room for two or more fins, and eliminating the second fin does not solve the problem. Raising the fin height to compensate for the lower breadth is likewise problematic. Furthermore, according to Ryckaert, having two fins helps compensate for process variability. Starting from 5 nm and below, the designers have to choose whether to use FinFETs, gate-all-around FETs (GAAFETs), or multi bridge channel FET (MBC FET). When the fin width reaches 3 nm, a challenge rises, a node-3 (N3) FinFETs may have just one fin; however, improving fin performance and eliminating parasites require sophisticated approaches. One way is to use Germanium for the p-channel and utilize high-mobility channels, but that comes with some integration challenges [27].

5.2. GAAFET and MBCFET

In general, GAAFET performs better than FinFET, as 3 nm GAA would have lower threshold voltage and (15-20) % power than 3 nm FinFET. However, GAAs and FinFETs still share similar back-end-of-the-line (BEOL) and middle-of-the-line (MOL) sections, which keep the performance enhancement about 8%. BEOL is one of the main steps of the semiconductor manufacturing process in which the inter-connectors are formed within the integrated circuit. These tiny metal wiring systems are becoming more crowded with each node down-scaling, causing more resistance-capacity (RC) delay in electronic chips [28].

5.3. NSFET/MBCFET

Scaling FinFETs will will soon come to an end, forcing chipmakers to apply alternative transistor technologies, such as nano-sheet FETs (NSFET). An NSFET is a FinFET on its side with a gate wrapped around it, and it contains several separated horizontal sheets that are vertically stacked, with each sheet containing a channel. A gate surrounds each sheet to form a gate-all-around transistor. NSFETs have been shown to have less RC latency than FinFETs [28]. NSFETs perform better and leak less since the current is controlled on four sides. NSFETs would typically have four sheets of (12-16) nm width, and a thickness of 5 nm. Wider sheets can pass more drive current. NSFET technology, on the other hand, still faces several hurdles, including n/p imbalance, gate length control, inter-spacer, bottom sheet efficacy, and device coverage [26]. However, when they are compared to nanowire FETs (NWFETs), NSFETs are more prone to fabrication process variations, such as those driven by line edge roughness (LER).

On the other hand, NSFETs are more immune against other process variations and showed less ON current mismatch than NWFETs, but the NWFET achieves a lower mismatch in DIBL and sub-threshold slope [30]. The advent of Samsung's multi bridge channel FET (MBCFET) at the 3 nm node marked the beginning of NSFETs in the industrial world. Some research centers, like IMEC, develop more advanced GAA forms, such as forksheet FET and complementary FET (CFET), targeted for 2 nm and beyond. A CFET is a complex version of GAA, while a conventional GAAs stack several p-type wires in one device and n-type wires in another, CFETs stack both n-FET and p-FET together to reduce the silicon area.

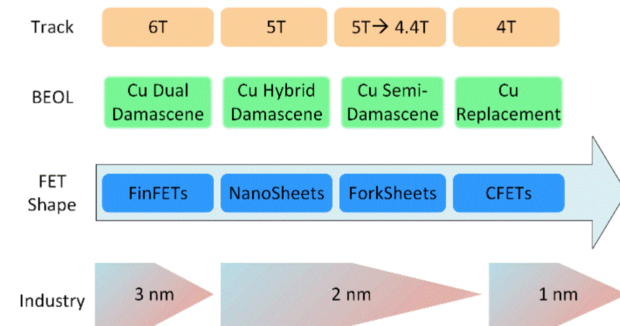

Fig. 2: MOSFET Technologies Roadmap

6. Discussion

IC manufacture has progressed in two ways throughout the years. The first is process improvement, which entails production on a smaller scale. Transistor channel length has dropped from a few um (micrometer) to a few nm through time (nanometer). Another type of enhancement is the structural level. The original transistor architecture, for example, was planar, but it has since been replaced with a tri-gate architecture, which has significantly superior gate control. In addition to breakthroughs in EUV lithography, Moore's Law cannot be sustained without advancements in FEOL device architecture. FinFET transistors have become the most popular transistor, with two fins in a 6-track (6T) standard cell. When FinFETs are scaled down to 5T standard cells, fin depopulation occurs, resulting in only one fin per device and a considerable loss in device performance per unit area. The footprint of vertically stacked nanosheet devices is smaller. Furthermore, using buried power rail (BPR) saves interconnect resources for routing, which helps to reduce the design area. At the cell level, CFETs leverage the third dimension by folding n-FETs over p-FETs or vice versa; this approach allows cells to scale down to 4T.

All these developments imply that the transistor density within an IC will keep following Moore's integration trend. Nevertheless, node-to-node performance increases at fixed power, known as Dennard scaling, will stagnate due to the inability to lower supply voltage further. 2D materials in the channel, such as tungsten disulfide (WS2), promise better performance since they allow more gate length scaling than Si or SiGe. A gate stack surrounds many stacked sheets and contacts them from the side. These devices, according to simulations, can outperform nanosheets at scaled dimensions approaching the 1 nm node or beyond. Beside FEOL, routing congestion and RC delay in the BEOL have become significant performance bottlenecks. In addition to FEOL, routing congestion and RC delay in the BEOL have become significant performance bottlenecks. We are looking into hybrid metallization with Ruthenium (Ru) or Molybdenum (Mo) to improve the via resistance. In the tightest pitch of the metal layers, semi-damascene metallization will simultaneously reduce resistance and capacitance. Furthermore, various alloys are explored to replace traditional copper wires for better properties. Other emerging system-level performance improvements exist, but they are outside the scope of this article, which focuses on the major trends in the semiconductor industry.

7. Conclusion

The electronic chips industry plays a significant role in shaping the future of technology, economics, and politics. The article discussed the latest achievements, trends, and forecasts of the semiconductors industry. It covered the latest semiconductor photo-lithography techniques, transistor structures, promises, and challenges. At the semiconductor processing level, extreme ultraviolet lithography (EUL) is the latest trend to manufacture sub 7 nm features, where the EUL short wavelength eliminates the need for multi-patterning. At the material level, the article briefed the most recent advances that aim to replace traditional semiconductor manufacturing materials to improve transistor performance. At the device architecture level, going below 2 nm features requires new transistor constructions, such as forksheet FET and complementary FET (CFET). The article also briefed other development trends at front-end-of-line (FEOL), middle-of-line (MOL), and back-end-of-line (BEOL) levels. New transistor architectures, materials, and fabrication techniques must all be developed to maintain Moor's rate of transistor integration.

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